REMARKS

Claims 1 - 20 were pending in the present application for patent as of the Office Action of February 23, 2005. In the Office Action of February 23, 2005, the Examiner rejected claim 1 under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention, rejected claims 1, 2, 19, and 20 under 35 U.S.C. 102(e) as being anticipated by US 2004/0266115, Chan et al. rejected claims 3, 4, and 12 - 14 under 35 U.S.C. 103(a) as being unpatentable over Chan et al. in view of US 2004/0117748, Tester, and objected to claims 5 - 11 and 15 - 18 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 1 was rejected under 35 U.S.C. 112, first paragraph. Claim 1 has been amended as indicated above in the complete claim listing. The applicants believe that claim 1, as amended, is allowable under 35 U.S.C. 112, first paragraph.

Claims 1, 2, 19, and 20 were rejected under 35 U.S.C. 102(e) as being anticipated by Chan et al. Chan et al. discloses a method of making a multiple gate electrode on a semiconductor device having a projecting fin, where the method controls the dimensions of the multiple gate electrode. Chan et al. controls the dimensions by planarizing the surface of the gate electrode material so that a patterned mask will lie flat on the surface. Chan et al. reports that this method positions the mask with the proper focus for patterning, thus ensuring precise dimensions.

Chan et al. does not show or suggest a method for converting a planar transistor design to a vertical double-gate transistor design as claimed in amended claim 1. As discussed above, Chan et al. discloses a method of making a multiple gate electrode on a semiconductor device. In the office action, the examiner appeared to suggest that the planarized gate electrode of Chan et al. is equivalent to the planar transistor design of claim 1. The applicants respectfully assert that the planarized gate electrode material of Chan et al. is not the same as the planar transistor design of claim 1. One example of a planar transistor layout is illustrated in FIG. 1 of the present application. Also, the examiner suggested that the interlayer 5 of Chan et al. is

equivalent to the intermediate layer of claim 1. However, the interlayer 5 is an insulating layer deposited on a silicon substrate, and is not "based on an overlapping region of the gate layer and the active layer" as claimed in amended claim 1. Also, as is clear from the context, the word "layer" of claim 1 refers to a set of coordinates and the word "layer" of Chan et al. refers to a material structure. In addition, Chan et al. does not show or suggest the first, second, or resulting layers of amended claim one. Further, Chan et al. does not show or suggest that the resulting layer is "for use in creating at least a portion of a mask" as claimed in amended claim 1. In Chan et al., the mask is used in the method of making a semiconductor device, and is not made from the method disclosed in Chan et al. Therefore, the applicants believe that amended claim 1 is allowable over Chan et al.

Claim 19 has been amended similarly to amended claim 1. Claims 2 and 20 have been amended to claim that the least one dimension comprises a spacing between the at least two fins. The applicants believe that the above comments regarding the rejection of claim 1 apply to the rejection of claims 2, 19, and 20, and that claims 2, 19, and 20 are allowable over Chan et al.

Claims 3, 4, and 12 - 14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. in view of Tester. Tester discloses a method for creating derivative semiconductor design layouts for closely related semiconductor designs in a product family. An exclusive OR (XOR) operation is used to add to or delete from a baseline layout while the baseline layout remains unchanged. As discussed above, Chan et al. discloses a method for making a multiple gate electrode on a semiconductor device. A combination of Chan et al. and Tester does not show or suggest the present invention as claimed in amended claims 3, 4, and 12 - 14. For example, neither Chan et al. nor Tester discloses or suggests a method for converting a planar transistor design to a vertical double-gate transistor design. Also, neither Chan et al. nor Tester disclose "defining a first intermediate layer based on an overlapping region of the gate layer and the active layer". Tester only discloses adding or deleting regions from a baseline layout using the XOR operation. In addition, neither Chan et al. nor Tester disclose "using the first intermediate layer to define a second intermediate layer, the second intermediate layer for defining at least one dimension of the vertical double-gate transistor design". Generally, claim 3 of the present application claims that defining the first intermediate layer comprises performing an AND function between the gate layer and the

active layer. The examiner stated that performing an AND function between an overlapping region between two layer regions is inherent in a layout software tool. The applicants respectfully assert that even if a layout tool can inherently perform an AND function, it is up to the designer as to what layers, or portions of layers, are combined using a logical function such as AND or XOR functions and what result is achieved. In addition, the applicants respectfully disagree with the examiner's assertion that Chan et al. discloses making a multiple gate transistor from a planar transistor. Chan et al. only discloses making a multiple gate transistor having a fin. Nowhere does Chan et al. disclose a planar transistor design or layout as claimed in the present application. Chan et al. only uses variations of the word "planar" to describe a characteristic of, or processing step to, a gate electrode material. Therefore, a combination of Chan et al. and Tester would only result in a method for making derivatives of a baseline layout by adding or deleting from the baseline layout, where the baseline layout includes a multiple gate transistor having one or more fins. For at least the above reasons, the applicants believe that claims 3, 4, and 12 - 14 are allowable over Chan et al. in view of Tester.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless the applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Believing to have responded to each and every rejection contained in the Office Action mailed February 22, 2005, the applicants respectfully request the reconsideration and allowance of claims 1 - 20, as amended herein; thereby placing the application in condition for allowance.

Respectfully submitted,

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